NORTHERN ARIZONA UNIVERSITY
College of Engineering, Forestry & Natural Sciences
SCHOOL OF INFORMATICS, COMPUTING AND CYBER SYSTEMS

DRAM Engineers
Northern Arizona University
620 S Knoles Drive
Flagstaff, AZ 86001

December 1, 2017

Daniel Eichenberger
Micron Technology
8000 S Federal Way
Boise, Idaho 83707

To Whom It May Concern:

All the team members are ecstatic to work on building a large scale DRAM model to emulate read, write, and refresh cycles and we all fully commit to finishing the project on time, in full operational state. The team would like to thank Dr. David Scott and Dr. Kyle Winfree, Daniel Eichenberger from Micron for sponsoring the project, and Julie Heynssens, our Faculty Mentor. The reason why all of us chose the Large-Scale DRAM project as out top choices, is because we are all experienced and knowledgeable in semiconductor physics and wanted the opportunity to apply our skills to a real-life application.

In the following sections of this paper, you will find our individual research topics as with our findings and references, as well as our requirements which were acquired from talking with our sponsor and from our research. Also included is a summary of our problem background and definition which explains why this project has been undertaken and our team's commitment to successfully complete the project by the end of our capstone course.

We are all very excited to work on this project. It combines all of our skills and knowledge from the last four years and applies it to create a real-time DRAM array model. Most of the members in the group intend to pursue a career in the semiconductor memory, so this is a great starter project to get us exposure to what those engineers have to think and be concerned with in their daily careers.

Sincerely,
Colby Weber
Demetria Shepherd
Zeyu Zhang
Jinming Yang
Abdulrahman Alqahtani

Large Scale DRAM Array Model

Sponsored by Micron Technology

“DRAM Engineers” Team Contact Information

Students:

Jinming Yang	jy345@nau.edu	(928) 679-5647
Zeyu Zhang	zz74@nau.edu	(928) 234-3593
Demetria Shepherd	dcs245@nau.edu	(602) 574-7045
Colby Weber	ccw95@nau.edu	(623) 628-8708
Abdulrahman Alqahtani	asa266@nau.edu	(202) 568-5218

Sponsor Mentor:
Daniel Eichenberger deichenberge@micron.com

Faculty Mentor:
Julie Heynssens julie.heynssens@nau.edu

Capstone Mentor:
Ashwija Korenda Ashwijakorenda@nau.edu

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1. Project/Problem Definition

Micron Technology is one of the largest companies that manufactures memory and enhancing storage devices. However, their technical expertise may be challenging to understand memory. To simplify their work, Micron Technology proposed to Flagstaff's NAU Electrical Engineering Capstone to design and build a large scale of Dynamic Random Access Memory Array, or DRAM Array. Today, there is no work or simple demonstration of how DRAM operates. Our Client, Daniel Eichenberger, is Micron's recruiter and test engineer, and desires a DRAM model to showcase the operation and basic fundamentals of memory.

This involves building the heart of the model, which is an eight-by-eight array of m-bit cells. The m-bit cell is a storage component to store small amounts of memory. In addition, the m-bit cell needs a refreshing cycle in order for memory to be retained. The refresh, read, and write cycles of DRAM are controlled by the peripheral circuits. The relevance of peripheral circuits is to ensure the proper operation of a DRAM.

An overview of the model's configuration is as shown in figure one. The application of building an interactive DRAM model helps Micron Technology display to employees their memory design and how it works in real time. This is in an effort to show potential recruits what they'll expect in DRAM manufacturing and testing. So to accurately who refresh, read, and write states, Light Emitting Diodes (LEDs) will be placed at the end of the storage capacitors which dim or brighten based on the state.

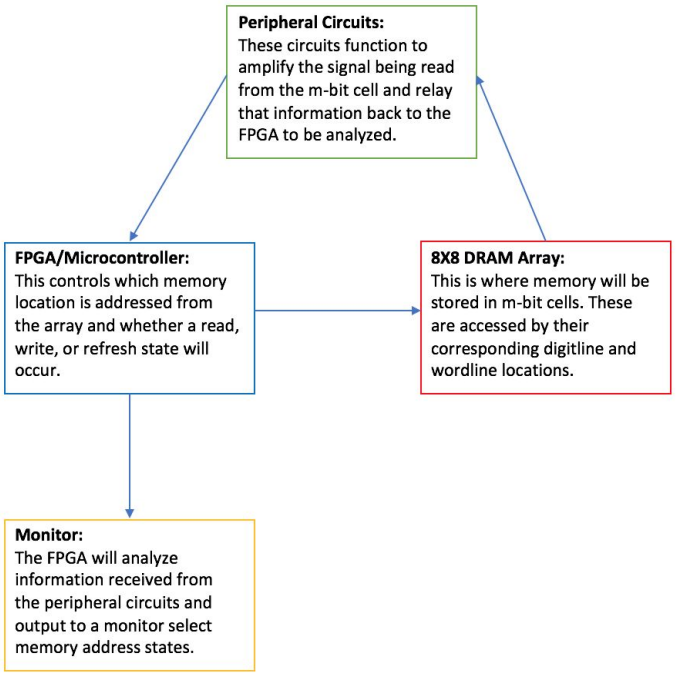

Figure 1: Simple diagram depicting layout and operation of the model.

So, as described to the team, the client wants a model of a DRAM array which can be shown to future Micron employees to give a sense of one of the company's products. It needs to be lightweight and small enough to carry with one hand, as well as reliable and durable as it will be handled by several different people. Using the DRAM model also needs to be easy to use so that any Micron employee, not just our client, can intuitively pick up the model and see how it operates.

2. General Research Survey Results

2.1 Internal and External Voltages

DRAM has a very high density, meaning it has a cheap data cache in computers. Also it must be periodically refreshed, making it slower than SRAM which does not require a refresh to retain memory. DRAM is volatile, meaning it is not ideal for program (long-term) storage [1].

2.1.1 Internal Voltage

The voltage between the transistors is $\frac{Vcc}{2}$. The reason is because the voltage needs to travel to either D1 ,and D1* (digitline or digitline not) to keep them at $\frac{Vcc}{2}$, after the signal has been read from the capacitor by the peripheral circuits [2]. The voltage between two internal points of an isothermal semiconductor device is not necessarily the difference between the quasi fermi levels because it can be zero; the voltage involves both the quasi fermi level and chemical potential differences in the internal circuit [3]. The internal circuit consists of two components: an emf source which is electromotive force and internal resistance [4]. So one of the functions of these peripheral circuits is to make sure the voltage on the digitlines remains at $\frac{Vcc}{2}$ so the memory stored on the m-bit cell can be most accurately read.

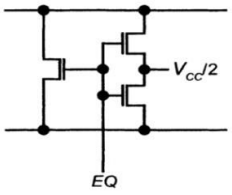

Figure 2: Equilibration schematic [2].

2.1.2 External Voltage

The external voltage consists of power between two external terminals that will be used to power the external components of the model like the FPGA (Field-Programmable Gate Array). The external voltage within the circuit is connected between the terminals of the power supply, including wires, resistors, lamps, and capacitors [4]. In order to write full V_{DD} (Voltage Drain Drain used for semiconductors) the max possible positive power supply voltage on the storage capacitor worldline must be $V_{cc} + V_t$ (Voltage Threshold) [2].

2.1.3 Reading and Writing from the Array

Part of Micron's project, the DRAM needs to read and write from the memory array. The array is constructed of an eight by eight m-bit array with gates on the word-lines and drains on the digit-lines. The read and write cycles depend on the clock's rising and falling edges of RAS (Row Access Select) and CAS (Column Access Select). The logic of the reading and writing values changes simultaneously because DRAM is "dynamic," which requires data to be refreshed every five to six milliseconds in order to keep data stored on the capacitor [5]. DRAM suffers from long access time and high energy overhead and since the pins on the processor chip are expected to not increase much, it will hit a memory bandwidth wall. Additional cells may be added to the array so that only relevant bit lines are read out [6].

2.2 Basic Operation and Fundamentals of a DRAM

The basic model of a DRAM operation contains a simple 1T1C (one transistor one capacitor) memory cell. To build upon the 1T1C schematic, this creates a m-bit memory cell and can be extended into a bigger array size. There are two different type of lines intersecting the 1T1C model, which are called digit-lines and word-lines. The "digit-lines" (bit-lines or column lines) are wired vertically and connected to the drain side of the transistor. On the other hand, "word-lines" (or row lines) are connected horizontally and to the gate side of the transistor [2]. The figure below is an example of a simple 1T1C memory cell, which was obtained from "DRAM Circuit Design Fundamentals and High Speed Topics."

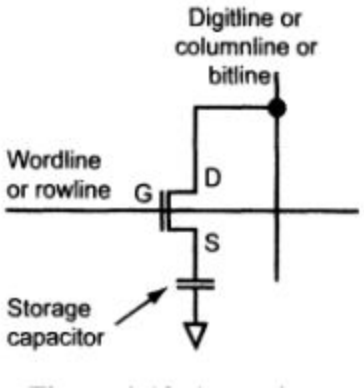

Figure 3: 1-transistor, 1-capacitor (1T1C) memory cell [7].

The digit-lines and word-lines are fabricated in metal, or polysilicon. Polysilicon is often used because this type of 1metal material helps activate the MOSFET (Metal-oxide Semiconductor Field Effect Transistor) to cross active areas [2]. The main purpose of the m-bit cell, it carries binary information when the capacitor charges and discharges to store information through the lines. Capacitors, however, can cause leakage due to the time of non-usage and the memory from the m-bit can lose information [7]. In order to prevent memory loss, a refresh cycle of the m-bit memory cell will be required to continue carrying binary information.

Part of the DRAM operation, it requires multiple pins such as address, command and data input/output. According to Micron's DDR3 SDRAM spec sheet, the row address

activates the basic commands and the column address pre-charges to READ/WRITE commands, then places the information into a memory cell bank [8]. The command pins are followed by the addresses depending on what information is being entered. Data input and output information enters in and out of the data bus. Also, clock signals count in real-time and at every positive clock edge from the signal.

2.2.1 Other types of Dynamic Random Access Memory

The 1T1C memory cell is not the only particular model to design a DRAM. There are two other types of DRAM designs operating the same technique as the 1T1C, which are three transistor model and one transistor with a diode.

2.2.2 Three Transistor Model

The three transistor model is built as from it's name, there are three transistors connected between the I/O lines and ground. For example, figure 4 demonstrates the model, which has two NMOS transistors in series and parallel to one NMOS transistor. The three transistor model is an interesting DRAM design, however, it does require a storage refreshing and leakage may occur due to the time of usage.

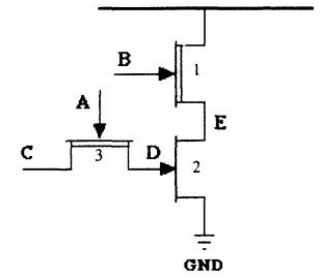

Figure 4: Three Transistor Memory Cell [9].

2.2.3 One-Transistor with a Diode Model

The one-transistor with a diode is slightly similar to the three transistor model. One of the transistors of this model, labeled number 1 from figure 5, acts like a capacitor and the transistor is non-active. On the other hand, the transistors below the "acting capacitor" transistor are treated as diodes, and activates as a reversed biased diode.

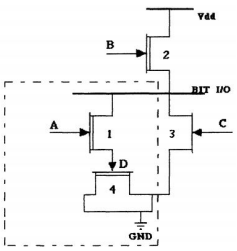

Figure 5: One Transistor with a Diode model [9].

2.3 Accessing the Array and Error Correction/Prevention

2.3.1 External Access to the Array

As mentioned in section 4.2 of the basic operation of DRAM, the m-bit cell is the main component in a DRAM array. The m-bit model is made by an NMOS transistor

which has its gate on the wordline, drain on the digitline, and source connected to the capacitor in which memory is stored in the form of charge [2]. The wordline applies a voltage to the gate of the selected NMOS to turn it on and to access the storage capacitor. The charge from the capacitor will travel through the digitline and can be read by being fed to the sense amplifier, which figures 6 and 7 exemplifies the sense amplifier [2]. Figure 6 shows how the sense amps are configured in between the m-bit arrays. Figure 7 shows the circuitry that goes into creating an efficient sense amp which detects small signals, amplifies them, then sends it down whichever digitline the amplifier is connected to.

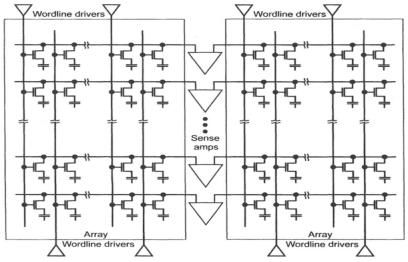

Figure 6: Open digitline array showing configuration of m-bits and sense amps [2].

The word-lines and digit-lines are helpful to rely on gaining external access to the DRAM model [2]. The digit-line will pick what m-bit cell we are trying to access and the firing word-line will turn on the selected transistors on that line [2]. The main plan is to implement this on a physical board. Tieing the word-lines and digit-lines can help separate busses and control the voltages of those busses from a computer board like a microcontroller or FPGA board (Field-Programmable Gate Array).

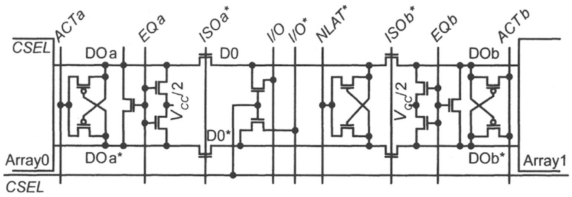

Figure 7: Schematic inside the Sense Amp circuit which amplifies the signal from the storage capacitor on the m-bit cell while maintaining a steady VCC/2 voltage on the digitline [2].

2.3.2 Modeling the m-bit

After researching a large scale DRAM array model, it was clear that no such model had recently created since DRAM can be made on a small PCB (printed-circuit-board). The capacitor will be sized based on the amount of charge we need to store which is given by equation 1 listed below [10].

$$Q = \frac{Vcc}{2} \times Capacitance$$

Equation 1: Q is the amount of charge that will be stored on the capacitor [2].

Based on the amount of charge to store on the capacitor, the size of the m-bit must maintain an operated input voltage at 1.2 Volts (in V_{CC}) [2]. From there we will

choose a transistor who operates at a voltage, which is V_{CC} – V_{th} (transistor threshold voltage, voltage consumed by the transistor). To store a full logic 1, +V_{CC} on the capacitor, the voltage needed on the wordline is V_{CC} + V_{th} to compensate for the voltage drop across the transistor which is V_{th} as shown in figure 8 [2].

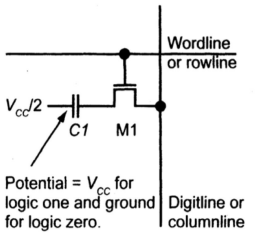

Figure 8: The process of storing a logic 1 or 0 on the storage capacitor C1 [2].

2.3.3 Refresh Cycle and Redundancy

One of the requirements of the project is to have the model emulate a refresh cycle, a mandatory action for a DRAM to retain its memory. The capacitor in each m-bit cell discharges at a slow rate over time, and it needs to be read every time. The READ places of the contents from the memory cell to the digitline, which is pulled to V_{CC} or to ground depending on the output of the sense amps. The DDR standard requires that every cell of DRAM refreshes within a sixty-four milliseconds interval [11].

In addition, redundancy within DRAM arrays have been used since the early days of the 256k generation. If there was any damages on a m-bit, redundant m-bit cells can replace address location of a poor m-bit cell [2]. Redundant cells come in handy save time and parts to repair the poor cells. Redundancy is also referred as to repair other elements, such as cells, word-lines, digit-lines [2].

2.4 The I/O process of DRAM

2.4.1 The Input process of DRAM

Input operation is divided into two cases, logic 0 and logic 1. However there still is one action before inputting data, the capacitor's original status may be at a high or low voltage. Inputting a logic 0 or logic 1 to DRAM, it may cause a different operation to happen in the m-bit cells. For the logic 0 case, the voltage on the I/O line is 0, the gate of MOSFET voltage will fluctuate from 5- to 0-Volts, and the voltage within the capacitor will decrease to very close to 0 Volts. At the beginning of the "write" operation of inputting the logic 1, the voltage on the I/O line is 5-Volts, the "gate" of MOSFET voltage will rise to 5-Volts, and the voltage in the capacitor will rise to close to 5-Volts, the "gate" voltage goes back to 0-Volts [2].

2.4.2 The storage process of DRAM

The voltage at the MOSFET "gate" is 0-Volts, so the charge does not flow from the capacitor and data can be saved. The 2.5-Volts is the reference demarcation line, if the capacitor's voltage is less than 2.5-Volts, the DRAM will save the input data as logic 0, or if the voltage is higher than 2.5-Volts, the data is saved as logic 1. The described conditions are only ideal, in physical applications charge in capacitor will leak. In other words, the number of electrons in capacitor will gradually decrease. The voltage will gradually increase and when the voltage rises to 2.5-Volts or more,

the data will be lost. So, the MOSFET must be open to charge the capacitor and make it keep its voltage. This process is known as the refresh cycle or refresh state [12].

2.4.3 The Output process of DRAM

The voltage of the I/O line will rise to 2.5V for inputting 0s, the gate's voltage will rise to 5V, the the capacitor's voltage will increase. The voltages on the capacitor and the I/O line become an intermediate value between 0-2.5V, closer to 2.5V (normally 2.3V). At this time, the inductive amplifier detects that the voltage on the I/O line is less than 2.5V, thus identifying 0 as the output. To output 1s, the voltage on the I/O line will rise to 2.5V, the gate's voltage will rise to 5V, There is a small increase of the capacitor's voltage because of the increase of voltage on the gate. It's hard to know the exact value, so normally you can assume 2.7V. At this time, the induction amplifier detects voltage on the I/O line is higher than 2.5V, identify 1 as output [13].

2.5 DDR Family and Comparison

The Double Data Rate Synchronous Dynamic Random Access Memory (DDR SDRAM), which is also known as DDR, is a kind of Random Access Memory with double memory block speed than Single Data Rate (SDR).

There are four primary parameters for DDR, which are memory clock, I/O bus clock, transfer rate and theoretical bandwidth respectively. The table attached below shows the popular designations of DDR modules (some was the old version but still popular at that time).

Name	Memory clock	I/O bus clock	Transfer rate	Theoretical bandwidth
DDR-200, PC-1600	100 MHz	100 MHz	0.2 GT/s	1.6 GB/s
DDR2-800, PC2-6400	200 MHz	400 MHz	0.8 GT/s	6.4 GB/s
DDR3-1600, PC3-12800	200 MHz	800 MHz	1.6 GT/s	12.8 GB/s
DDR4-2400, PC4-19200	300 MHz	1200 MHz	2.4 GT/s	19.2 GB/s
DDR4-3200, PC4-25600	400 MHz	1600 MHz	3.2 GT/s	25.6 GB/s

Table 1: Some Examples of Popular Designations of DDR Modules [14].

The table explains there are four generations of DDR family in total. With the generation updating, the I/O bus clock, transfer rate and theoretical bandwidth have the evident improvement. Especially the data in the transfer rate and theoretical bandwidth of latest versions, has increased to 6 times of the first version. Inversely, the memory clock has not changed as much.

2.5.1 DDR Third Generation

DDR3 is the third generation of the DDR family. Comparing to the DDR2, the 3rd generation reduced the power usage because of the low voltage (1.3-Volts or 1.5-Volts on DDR3 and 1.8-Volts or 1.9-Volts on DDR2). In addition, the data transfer rate of DDR3 is twice of DDR2 and four times of the first generation of DDR [15].

2.5.2 DDR Fourth Generation

DDR4, released in 2014, is the latest generation of DDR family. The frequency (800-2133 MHz) is twice than DDR3 and operates the lower voltage (between 1.2-Volts and 1.4V) [16]. Like today, many DDR4 is often used in PCs and smartphones.

2.5.3 Advantages of DDR4

To talk about the advantages of DDR4, the chip is more energy-efficient which is activated with 1.2-Volts less than voltage in DDR3 (1.5-Volts). If in the low voltage working state, the DDR4 will work with only 1.05V and DDR3 is 1.35-Volts For the data rate, DDR4 totally beats DDR3 with at most 3200 Mb/s. In addition, the DDR4 also has the larger DIMM capacities because of bigger chip density [17].

3. Requirements and Specifications

3.1 Mechanical

The size of the DRAM array has been proposed to be an 8X8 array of m-bit cells which are chained with their gates on the wordlines and drains on the digitlines. The entire model needs to be mobile and portable. The client requests that we make it small enough so that he can easily carry it with one hand, while being large enough to point out the individual circuits of the array.

- Size: The size of the DRAM size will be a 8x8 array of m-bits.
- Weight: Between 0 to 5 lbs.
- Organization: 8X8 m-bit array layout.
- Package: Small enough to carry with one hand.
- Protection: Model needs some sort of metal or wooden board to be constructed on so that a small drop or fall from table height would not severely damage the array.

3.2 Electrical

The model needs to be able to be powered by a standard receptacle, 208Y/120V and without the need to be reprogrammed every time for operation. So, to accomplish both those tasks a programmable microcontroller or FPGA will be used to control the voltages sent across the wordlines and digitlines. The maximum voltage required will be approximately 2V (just an estimate since exact parts have not yet been decided upon).

- Power: The model will have a relatively small current but the voltage applied to the wordlines will approximately be 2V.
- Accuracy: The model needs to be accurate enough to show charge, discharge, and refresh cycles on individual m-bit cells.
- Interfacing: The m-bits will be accessed by the wordlines which are controlled by the user on the FPGA or microcontroller.
- Aging: The client would like to be able to show this model at the Fall 2018 Career Fair for CEFNS majors so the model needs to be able to withstand at least 6 months of use. Our goal is at least a year in operation without major failure.

3.3 Environmental

The client has expressed that the model will be used indoors only and will be stored in a climate controlled room (between 70 to 85 degrees Fahrenheit). So, factors such as humidity, rain, and snow are not a concern. The model does need to be able to being transported in a vehicle so it should be able to withstand small vibrations and bumps. It also needs to withstand the fall from table height without showing signs of major failure.

- Temperature: Will be stored and used in a climate controlled room (70 to 85 degrees Fahrenheit).
- Vibration, shock: The model needs to withstand minor bumps and vibrations from transport as well as being able to withstand a fall from table height.

3.4 Documentation

The client has yet to specifically ask for a user's guide or reference manual but it is the consensus of the group that there should be some documentation on how to operate the model. A maintenance manual will also be provided on how to remove and replace certain components so that the model can be modernized and bad components can be replaced.

- Operator's/Maintenance Manual: A operator's manual on how to work the DRAM model will be provided along with a maintenance guide.
- Programming Languages: The code will be written in either C or VHDL. Once the program is written, they will be compiled and programmed to the microcontroller.

3.5 Software

No specific software was suggested by the client. He expressed to us that whatever programming language the group feels most comfortable in is the one that the team should use to program the controller for the wordline and digitline voltages.

- Programming language: C and VHDL are the preferred languages to code a microcontroller or FPGA.
- Software required to use: Pyxis Mentor Graphics will be used to simulate the circuit before building it. When programming the controller we will either use Arduino Genuino or Quartus Prime.

3.6 General

The client expressed no preference to controller manufacturer type or the brand of the electrical components such as for the capacitors and MOSFETs. For this information we will discuss with our faculty mentor Julie Heynssens as to what specifications to look for when selecting parts for m-bit operation. The client did say that he wanted the board to be reliable and function as expected when he demonstrates it to prospective employees. He also needs all of the components on the model to last at least until the Fall 2018 Career Fair.

- Reliability: Needs to power on and function as expected for at least 6 months.
- Vendor Preference: No vendor preferences currently.
- Client Preferences: No client preferences currently.
-

4. Project Breakdown

From the overall research, needs/requirements, and constraints provided by the client, we've broken down three major subsystems for the DRAM model: a required GUI (Graphical User Interface), a convenient microcontroller, and the large array size. Our main goal is to keep the model as simple and intuitive as possible. The GUI works like a control unit, by taking input from the user as to what m-bit cell to access, then sending the input to the microcontroller. It will also display information from the accessed m-bit cell, fed back from the microcontroller. The microcontroller takes input commands from the GUI and accesses the desired storage cell. Then, it will either perform a read/write operation, reading data stored or writing new data into that cell. The microcontroller is ideally able to display the read information via an HDMI cable to any monitor. The array is the layout of 8X8 m-bits (64 in total) is arranged, each cell being able to store charge for a noticeable amount of time as displayed by LEDs connected in parallel with the capacitors.

4.1 Subsystems

In this section, there are three major components broken down for the large scale DRAM model: the Graphical User Interface (GUI), Microcontroller, and DRAM Array. Figure 9 is a diagram to exemplify the flow of the three subsystems.

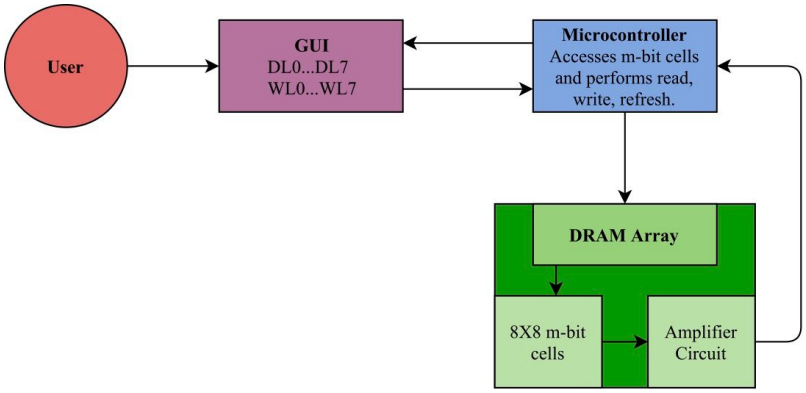

Figure 9: System flow diagram.

4.1.1 GUI

The GUI is a controller which takes input from user to select the desired m-bit cell. The GUI tells the microcontroller what m-bit cell to access and what operation will be performed, either a read or write. The GUI is based on the software, Processing. The reason why we chosen processing to design our GUI is that the programming languages (python or java) make it easy to design a good GUI, more importantly, these languages have a strong library to support the serial port communication between the PC (personal computer) and the microcontroller. MATLAB and Blynk were also considered as options to create the GUI but both were incredibly complicated, whereas a prototype GUI was developed in Processing in an hour.

The serial port communication is main way how the microcontroller communicates with other devices. To read information, GUI will send a signal variable to the microcontroller. The microcontroller will perform its read function which has been loaded on the board. Then, it will read information from the m-bit and transmit the information to the GUI through the serial port which is connecting the microcontroller and computer. To writer information, the user will input data and choose what m-bit cell to access through GUI. Data will be transmitted in an inverse procedure of the reading process.

4.1.2 Microcontroller

The Microcontroller will receive a control input signal from the GUI, instructing it to access a selected m-bit cell. Then it will either write information to that cell or send the signal already stored on the cell to the GUI so it could be displayed . Three major operations are performed by the microcontroller which are read,

write, and refresh. The microcontroller will apply a voltage to the correct digitlines and wordlines to access the user's desired m-bit cell. For reading the information, a pin will be connected to the capacitor from the microcontroller and read the information stored. For writing the information, a pin will be connected to the drain side of the transistor (digitline) and a voltage signal will be applied.

In selecting a microcontroller, three different board were considered. Those being the Arduino Uno, Raspberry Pi, and Altera Cyclone V (an FPGA which can function as a microcontroller). The Altera board was a strong contender as it provided the functionality required and also provided great external access to the array with built-in switches buttons, but it was far too expensive and well above our $100 budget. The Arduino Uno and Raspberry Pi are very similar. Both can perform functions needed to simulate DRAM operation, but the Raspberry Pi has an HDMI out which can easily display information from the array to a monitor and is only $10 more than the Arduino Uno. So the Raspberry Pi was selected as the choice of microcontroller.

4.1.3 DRAM Array

There are three main components of building the DRAM array, which are the following: transistors, operational amplifiers, and capacitors. Each component explains and mentions what specific part(s) will help corporate the requirements of this DRAM design.

Transistors: A transistor is a semiconductor device that acts like a switch and helps amplify signals. Our main goal for this transistor is to regulate signals and data going through the digitlines and wordlines. The main transistor, part number 2N7008, is what may be used to create the m-bit memory cells. Again, the m-bit cell contains 1T1C, one-transistor one-capacitor. The "source" side of the transistor will be connected to the wordline, "drain" side connects along with the capacitor, and the "gate" connects to the digitline. The 2N7008 transistor has been tested and implemented with other electrical engineering projects, and the performance of this transistor is greater than the other considered transistors, ZTX449 and 2N3004.

Operational Amplifiers (known as Op Amps): After testing the charge stored in capacitor, it is not enough to show a visible state of discharge as the LEDs fade too quickly. According to the formula of charges in a capacitor (Q = CV), to increase the charge in capacitor, you must increase capacitance or voltage. If the input voltage is higher than the LEDs and transistors maximum bearing voltage, the LEDs and transistors would burn up and become inoperable. In that case, the ideal way is to increase the capacitance. However, this project asks for a small size of DRAM array and large capacitance comes at a cost of a large sized

capacitor, which would dissatisfy the mechanical requirements. By considering the above conditions, providing a high voltage only to the capacitors is the most suitable choice. Therefore, the Op Amp is connected with the capacitor to amplify the input voltage and with the LED connected in parallel, using a large resistor to protect the LED. So, the charge in the capacitor is increased yet the transistor and LEDs still see a low voltage.

The TL082 Op Amp is the selected amplifier for this project. It was compared against the LM741 and TL081 but since both of these packages only have one Op Amp and the TL082 has two per package, it was chosen over the other two options. Also, the TL082 is a commonly used Op Amp in the students digital and analog design courses, so the students are most familiar with it.

Capacitors: The main function of the capacitors is to store the analog signal which is coming from the microcontroller and provide a space for the exchange of information. In view of the size requirement and budget, the electrolytic capacitor with the value should be in between of 4.7 microFarads and 2.2 milliFarads were selected. Super and Ceramic capacitors were also considered but the supercapacitors were far too expensive (averaging $2 per cap) which would have led the team to spend the entire $100 budget on capacitors. The Ceramic cheap like electrolytic but are more often used in resonant circuit applications to counter reactive power produced by the inductance.

5. Conclusion

By integrating all the components and implementing from our previous research, the “DRAM Engineers” team is on track to successfully emulate the operations of DRAM using a simple 8X8 array of individual m-bit cells, a microcontroller, and a graphical user interface (GUI). The m-bit cells consist a combination of the 2N7008 transistors, electrolytic capacitors, and TL082 Op Amps. The Raspberry Pi 3 Model B is the official microcontroller to use because of its large memory, programming language in Python, and the flexibility to show outputs on any monitor via an HDMI cable. Processing 3, the GUI for the DRAM, is the control unit and to accept user input. Combining both the user interface and microcontroller implementation, the m-bits will receive the signal sent from the user via the GUI and the Raspberry Pi will provide feedback information from the array to the GUI.

Again, Daniel Eichenberger from Micron Technology requested an assemble DRAM model and portable to show potential Micron interns and employees of the company’s memory and storage devices. The large scale DRAM model does require to show the read and write cycles, and provide some external access to the m-bit cells.

This report is to inform Micron of the team’s progress, including our individual research findings and our strategy to successfully complete the project.

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